REMARKS

Claims 1-13 were previously pending in this application.

Claims 1-13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Maniar et al., US Patent No. 5,702,981.

Claim 1 is amended to clarify the patentable subject matter of the present invention.

Claims 2 and 11-13 are amended to correct a grammatical error.

New claims 14-18 are added.

No new matter is added.

Claims 1-18 remain in the case.

Applicants request reconsideration and allowance of the claims 1-18 in light of the following remarks.

Claim Rejections – 35 USC § 103

Claims 1-13, are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,702,981 issued to Maniar et al. ("Maniar").

The rejection is respectfully traversed.

Claim 1 is amended to recite:

"forming plural interconnection layers, each including a capping layer, the capping layer defining a contact resistance, and an etching stopper, on a semiconductor substrate;

forming an interlayer insulating layer overlying the plural interconnection layers;

forming first contact holes in the interlayer insulating layer, thereby exposing a surface of the etching stopper;

removing a portion of the etching stopper exposed by the first contact holes, thereby forming second contact holes, to leave the capping layers of the plural interconnection layers at substantially the same thickness such that the contact resistances of the plural interconnection layers are substantially uniform; and

forming a conductive layer within the second contact holes." (Emphasis added)

None of the cited references teaches or discloses the above-recited features of claim 1. Rather, Maniar teaches away from the claimed invention because it even suggests that any capping layer that may be present in the interconnect can also be removed. See col. 5, line 66 – col. 6, line 4 of the Maniar reference.

To help explain the above points and the differences between the claimed invention and the Maniar reference, the following comments are further provided.

The claimed invention is directed to substantially reducing variations in the contact resistance between a plurality of interconnections. The claimed invention accomplishes this by forming first contact holes by stopping etching of the interlayer insulating layer at the etch stopping layer, and forming second contact holes by etching the capping layer exposed in the first contact holes to a certain degree. The thicknesses of the capping layers that remain in each of the second contact holes are, therefore, uniform. Consequently, the variations in the contact resistance between the plurality of interconnections can be substantially reduced.

However, the Manier reference is directed to minimizing the reaction between an interconnection and a source gas, which is used to deposit a conductive material in a contact hole by preventing the interconnection from being exposed to the source gas, even when misalignment between the contact hole and the interconnection occurs. To accomplish this, the Manier reference proposes to form an etch stop layer, which covers the top and sidewalls of the interconnection and a substrate and then to form the contact hole with the etch stop layer remaining on the sidewalls of the interconnection.

In the Manier reference, however, the capping layer remaining in the contact hole is removed in consideration of forming a barrier layer later. Thus, the interconnection layer is exposed until the barrier layer is formed. The examiner says that it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to leave the capping layer from the first deposition instead of etching the layer and re-depositing it in order to save manufacturing time. However, if the interconnection layer is exposed by removing the capping layer, as the Manier reference teaches, the interconnection layer reacts with outwardly diffused oxygen components in the interlayer insulating layer and a high resistive oxide layer is formed on the interconnection layer. This is contrary to the teachings of the present invention, which leaves the capping layers in uniform thicknesses in the contact holes to substantially reduce variations in the contact resistance between the plurality of interconnections.

For the reasons discussed above, the rejection does not present a *prima facie* case of obviousness. Accordingly, claim 1 is allowable. Also, claims 2-15, which depend from allowable claim 1 and recite features that are not taught or disclosed in the cited references, are allowable. For example, none of the cited references teaches or suggests "the capping layers are etched to form a uniform thickness among the second contact holes," as recited in new claim 14.

Similarly, new claim 15 recites:

"forming plural interconnection layers, each including a material layer comprising a capping layer and an etching stopper, on a semiconductor substrate;

forming an interlayer insulating layer overlying the plural interconnection layers;

forming contact holes to expose a surface of the etching stopper in the interlayer insulating layer;

selectively removing the material layer within the contact holes in such a manner that the capping layers within the contact holes are of uniform thickness; and

forming a conductive layer within the contact holes." (Emphasis added)

For the same or similar reasons discussed above, none of the cited references teaches or discloses the above-recited features of new claim 16. Particularly, nowhere does the Maniar reference teach or suggest "*selectively removing the material layer within the contact holes in such a manner that the capping layers within the contact holes are of uniform thickness.*"

Thus, new claim 16 is allowable. Accordingly, new claims 17-18, which depend from allowable claim 16 and recite features that are not taught or disclosed in the cited references, are also allowable.

For the foregoing reasons, reconsideration and allowance of claims 1-18 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Once amended) A method for manufacturing a semiconductor device comprising:

[sequentially] forming [an] plural interconnection layers, each including a capping layer, the capping layer defining a contact resistance, and an etching stopper, on a semiconductor substrate;

forming an interlayer insulating layer overlying the plural interconnection layers;

forming [having a] first contact holes in the interlayer insulating layer, thereby exposing a surface of the etching stopper [formed of a material having a high etching selectivity with respect to the interlayer insulating layer];

[forming a second contact hole to substantially expose a top surface of the capping layer by] removing a portion of the etching stopper exposed by the first contact holes, thereby forming second contact holes, to leave the capping layers of the plural interconnection layers at substantially the same thickness such that the contact resistances of the plural interconnection layers are substantially uniform; and

forming a conductive layer within the second contact holes.

2. (Once amended) The method for manufacturing a semiconductor device of claim 1 further comprising forming [a] third contact holes by slightly etching a portion of the capping layer exposed by the second contact holes before forming [a] the conductive layer, and wherein the conductive layer is formed within the second contact holes and the third contact holes.

11. (Once amended) The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is formed only in the second contact holes.

12. (Once amended) The method for manufacturing a semiconductor device of claim 1, wherein the conductive layer is an upper interconnection layer filling the second contact holes and covering the top surface of the interlayer insulating layer.

13. (Once amended) The method for manufacturing a semiconductor device of claim 1, wherein the first contact holes are [is] formed by using a dry etching method.

Claims 15-18 are new.